IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application	PATENT APPLICATION
Inventors: Adrian J. Isles	
Application No.: 09/586,191	Art Unit: 2123
Filed: June 2, 2000	Examiner: Sharon, Ayal I.
Title: CIRCUIT-LEVEL MEMORY AND COMBINATIONAL BLOCK MODELING	Customer No. 28554

DECLARATION OF RAJEEV MURGAI UNDER 37 C.F.R. §1.132

I, Rajeev Murgai, hereby declare:

1. I am a co-author of the article entitled "Logic Synthesis for Programmable Gate Arrays," 27th ACM/IEEE Design Automation Conference, ACM Press, 1990 ("*Logic Synthesis article*").

2. I received a Bachelor of Technology in Electrical Engineering from Indian Institute of Technology, New Delhi, India in 1987, a Masters of Science in Electrical and Computer Engineering from Carnegie Mellon University, Pittsburgh, PA in 1989, and a Ph.D in Electrical Engineering and Computer Science from University of California, Berkeley in 1993.

3. After graduating from University of California, Berkeley, in 1994 I began working at Fujitsu Laboratories of America, Inc. as a member of the research staff. In 2001, I became a part-time employee at Fujitsu Laboratories of America, Inc. and a part-time consultant with Zenasis Technologies, Inc. Since 2004, I have been employed full-time at Fujitsu Laboratories of America, Inc. My current job title is Research Fellow and my responsibilities include research, development, and project leadership in the area of Electronic Design Automation.

4. I am not employed by Averant, Inc. I do not own any stock in or have any financial interest in Averant, Inc.

RM/Aug 24, 2004

5. I am not receiving any compensation for providing this declaration.

6. My comments in this Declaration pertain to factual matters as understood by me.

7. The *Logic Synthesis article* is directed to logic synthesis for programmable gate array architectures (PGAs). More particularly, the *Logic Synthesis article* is directed to automatic tools that take a high-level description (such as Boolean logic equations or a Hardware Description Language such as Verilog or VHDL) of a combinational logic circuit and synthesize that logic onto a programmable gate array architecture based on the description.

8. Logic synthesis is part of the electronic design automation (EDA) field.

9. Programmable gate arrays are physical structures. The basic PGA architecture usually consists of repeated arrays of identical logic blocks. One category of these logic block arrays is called Table Look-Up and the resulting architecture is called a Table Look-Up architecture.

10. The portions of the *Logic Synthesis article* pertaining to Table Look-Up architectures are directed to the realization of logic functions using these architectures by using automatic tools to synthesize descriptions of the combinational logic functions onto the physical structures.

11. The portions of the *Logic Synthesis article* directed to the Table Look-Up architecture are not related to the problem of modeling memories (e.g., a random access memory), or modeling uninterpreted combinational blocks (i.e., so called "black boxes" which are combinational blocks whose inputs and outputs are given but whose functionality is undefined). Rather, the Table Look-Up is the actual physical structure onto which such an electronic circuit design can be logically synthesized.

12. The *Logic Synthesis article* does not disclose that equations or VHDL are used to model a Table Look-Up used in a programmable gate array.

13. The *Logic Synthesis article* is not directed to, nor does it disclose, the use of lookup tables (or any other technique) for modeling or representing memories (e.g., RAMs) appearing in electronic circuit designs. In particular, the work in the *Logic Synthesis article* does not address how memories appearing in electronic circuit designs can be modeled for efficient simulation and or verification in an EDA tool.

14. The *Logic Synthesis article* is not directed to, nor does it disclose, the use of lookup tables (or any other technique) for modeling or representing uninterpreted combinational

RM/August 24, 2004.

blocks of electronic circuit designs in descriptions of the electronic circuit designs.

15. The *Logic Synthesis article* is not directed to, nor does it disclose, replacing a portion of a description of an electronic circuit design with a lookup table, wherein the portion of the description relates to a memory (e.g., RAMs), and wherein the lookup table in the description represents the memory.

16. The *Logic Synthesis article* is not directed to, nor does it disclose, replacing a portion of a description of an electronic circuit design with a lookup table, wherein the portion of the description relates to an uninterpreted combinational block, and wherein the lookup table in the description represents the uninterpreted combinational block.

17. The *Logic Synthesis article* is not directed to, nor does it disclose, methods for using lookup tables to model memories in hardware description language-based descriptions of electronic circuit designs.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under §1001 of Title 18 of the United States Code and such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Executed in Sunnyvale, California, on August 24, 2004.

Rajeev Murgai

Rajeev Murgai